Patent Application Publication Sep. 25, 2008 Sheet 1 of 4 US 2008/0232504 A1

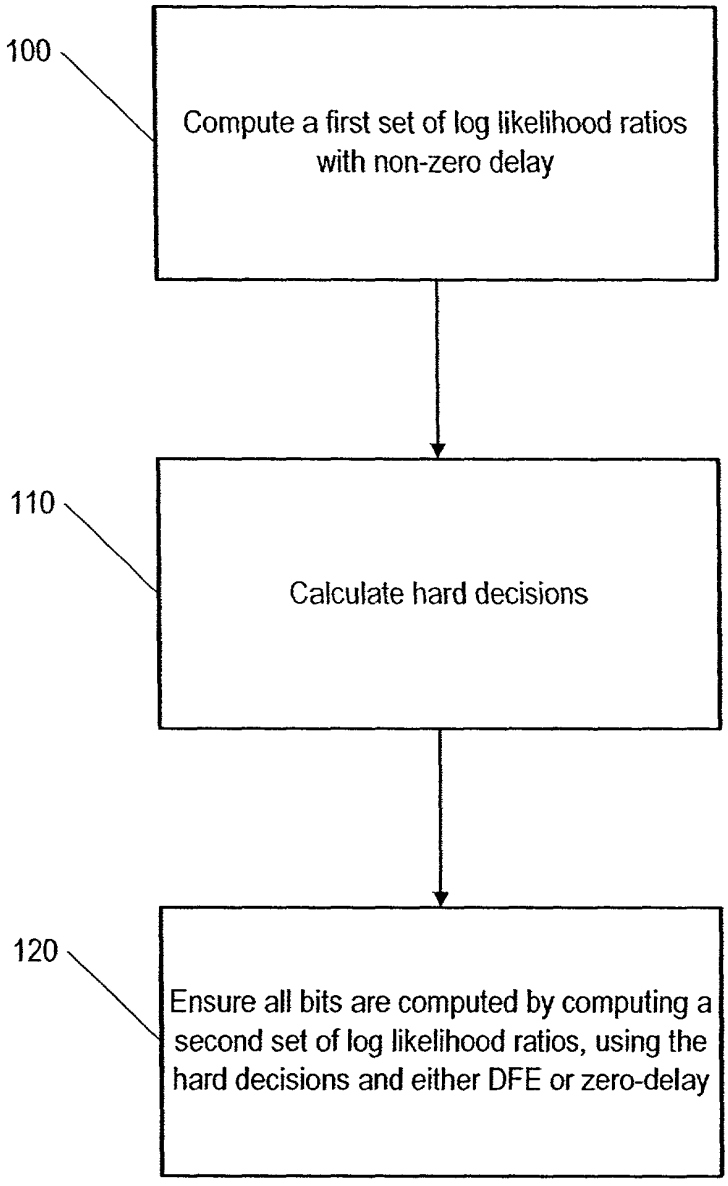

FIG. 1

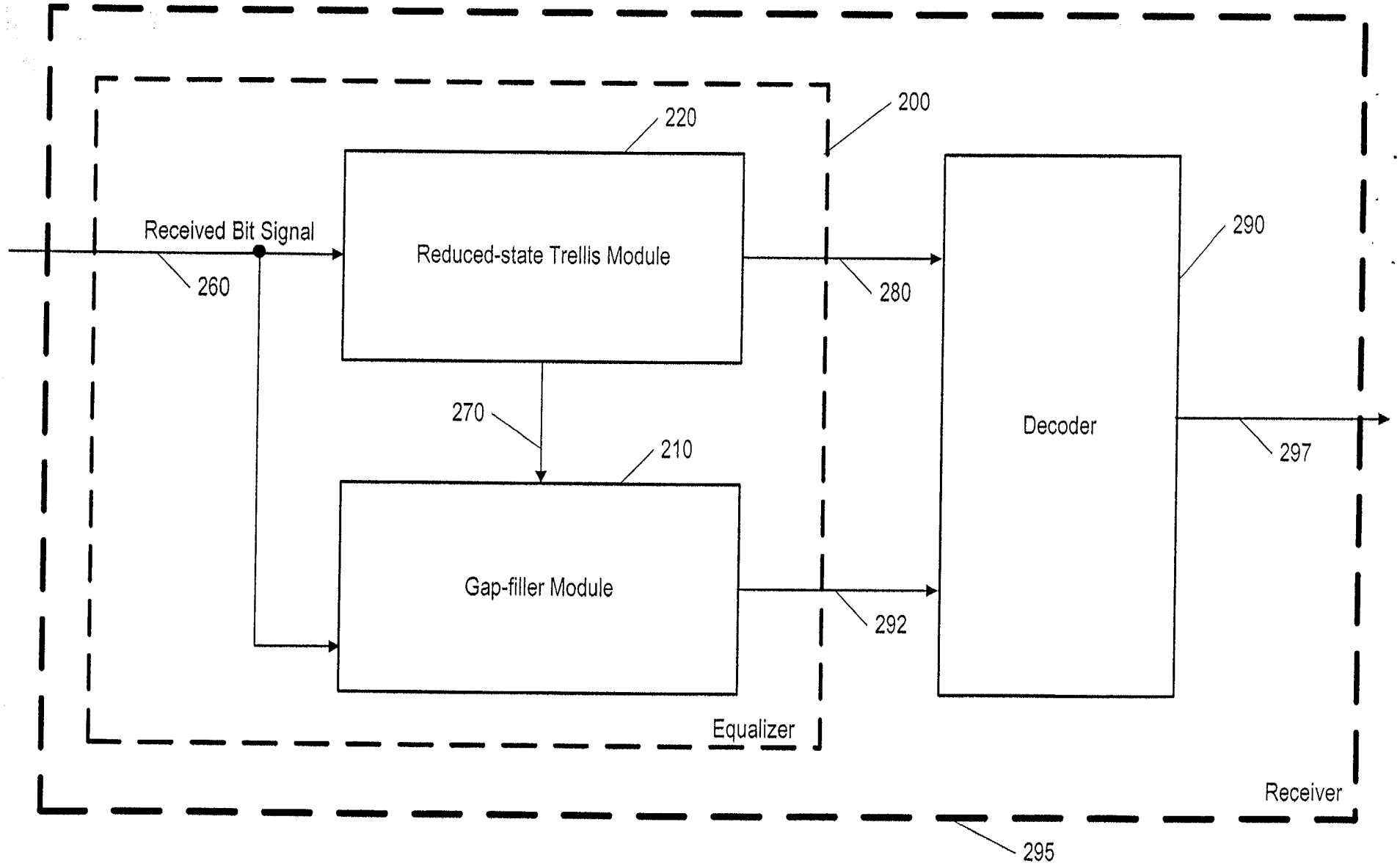
200
220
Received Bit Signal
260
Reduced-state Trellis Module
280
290
270
210
Decoder
297
Gap-filler Module
292
Equalizer
Receiver
295

FIG. 2

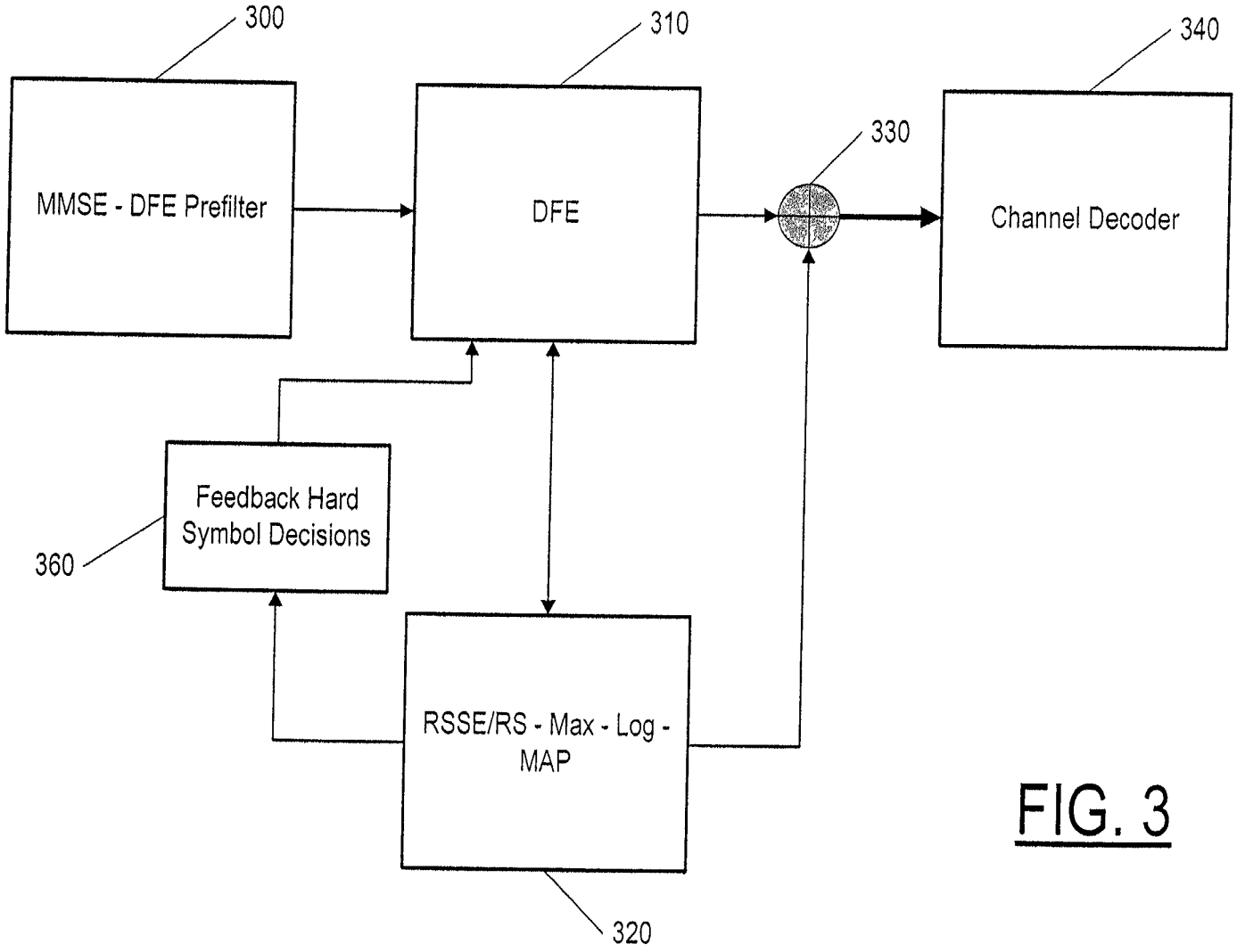
300
310
340
330
MMSE - DFE Prefilter
DFE
Channel Decoder
Feedback Hard Symbol Decisions
360
RSSE/RS - Max - Log - MAP
320

FIG. 3

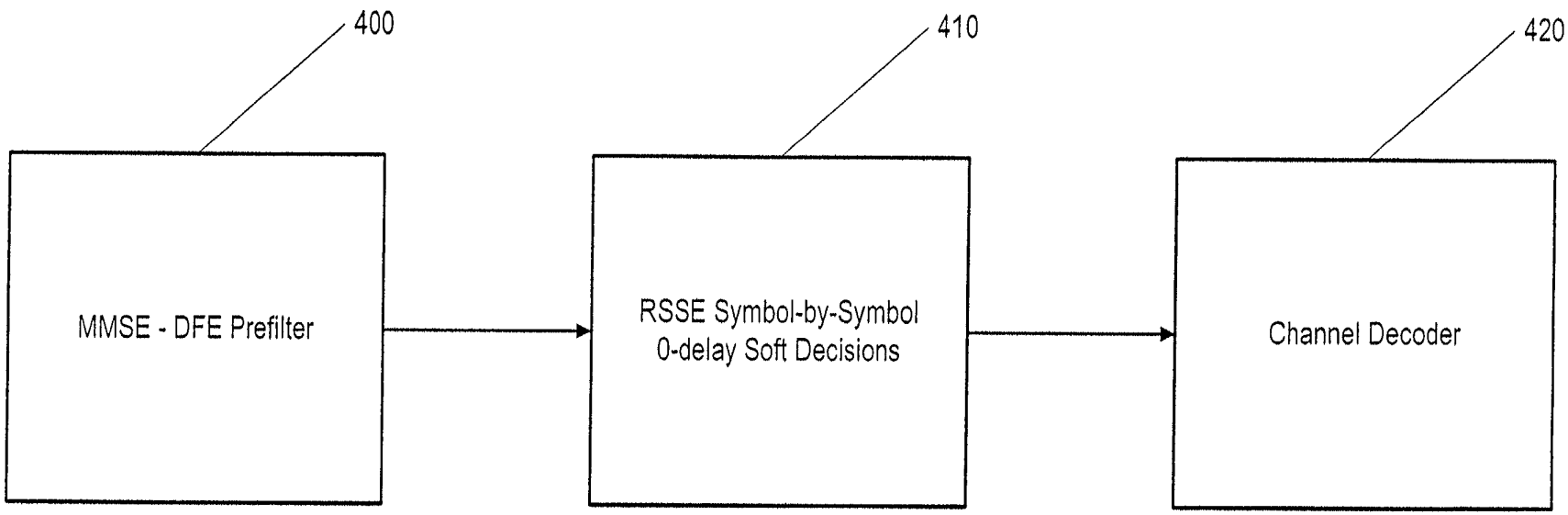
400
410
420
MMSE - DFE Prefilter
RSSE Symbol-by-Symbol
0-delay Soft Decisions
Channel Decoder

FIG. 4

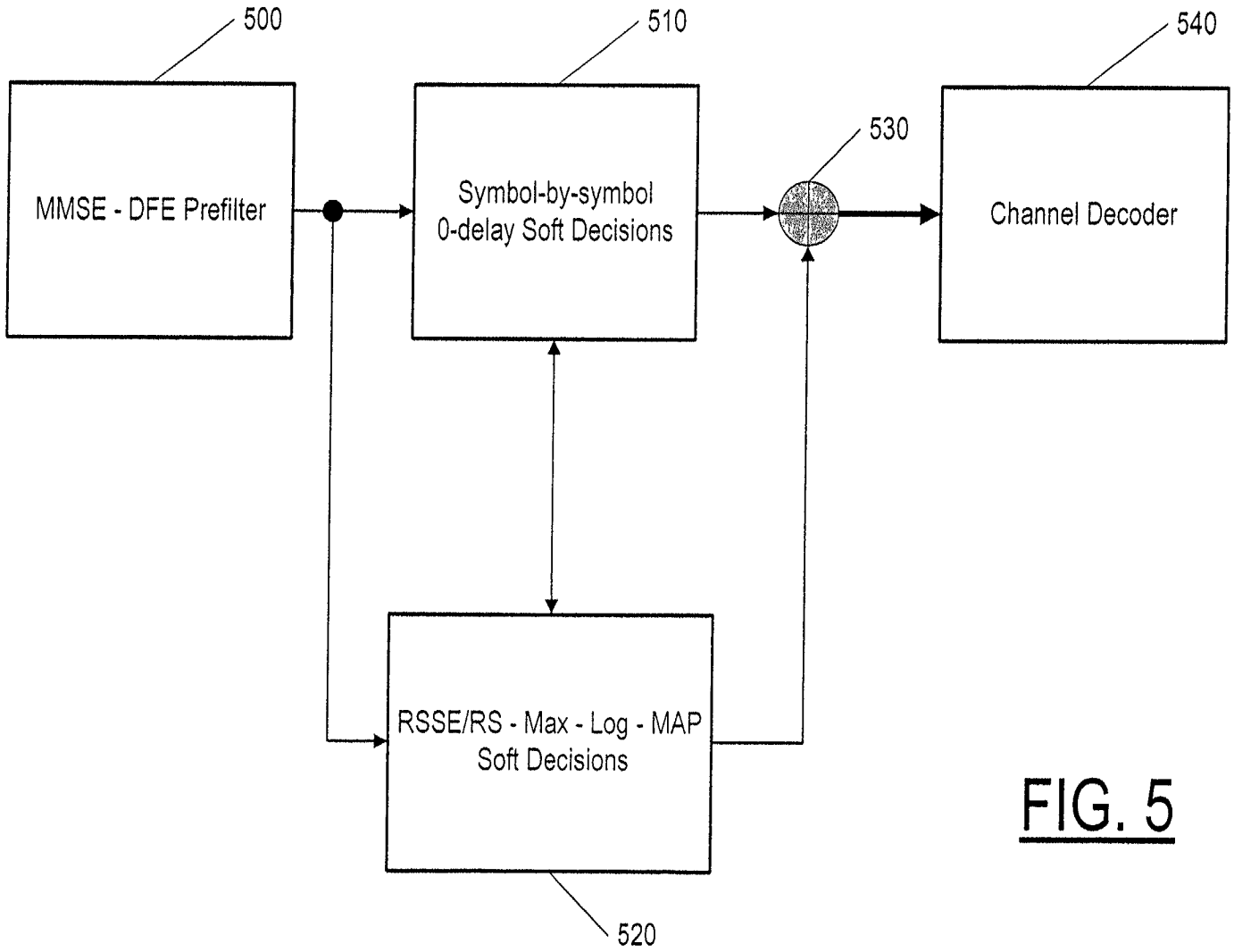
500
510
540
530
MMSE - DFE Prefilter
Symbol-by-symbol
0-delay Soft Decisions
Channel Decoder
RSSE/RS - Max - Log - MAP
Soft Decisions
520

FIG. 5

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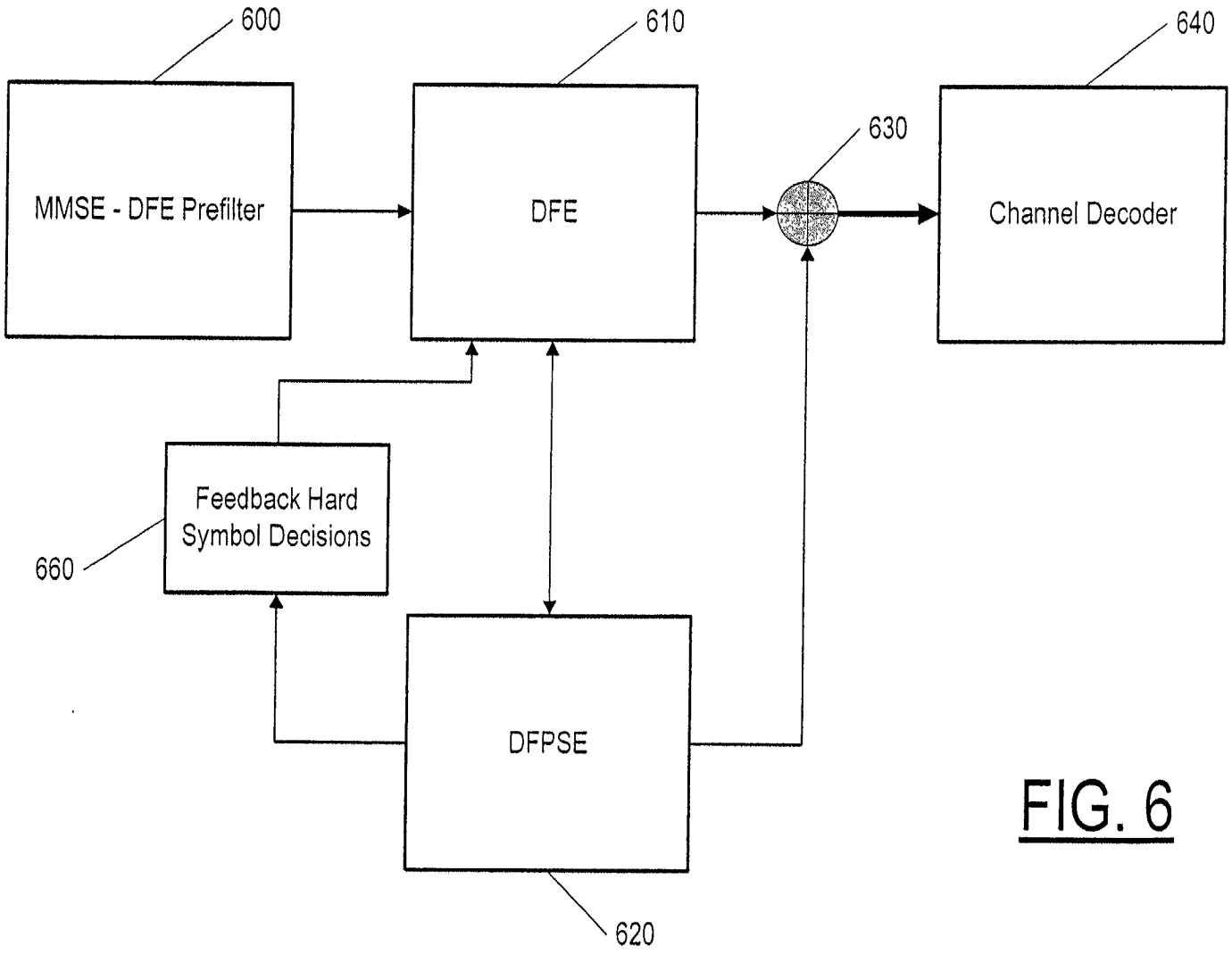
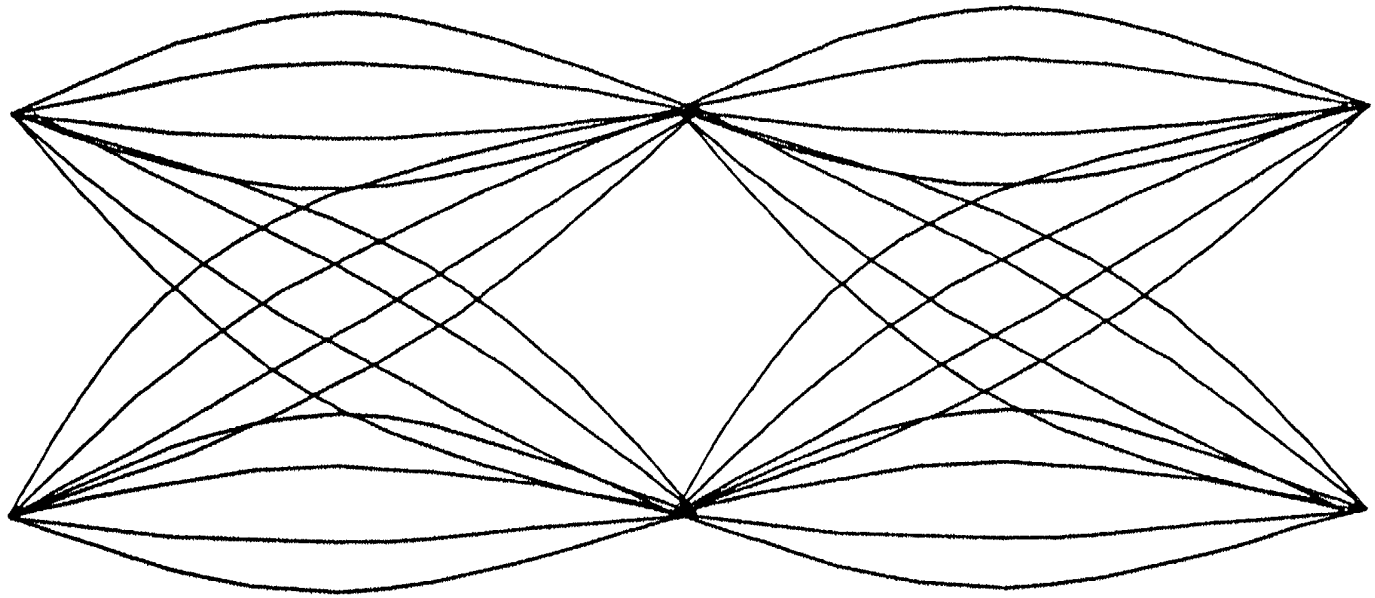


FIG. 6

$S_k = \hat{a}_{k-1}$ a_k $S_{k+1} = \hat{a}_k$ a_{k+1} $S_{k+2} = \hat{a}_{k+1}$

A = {0 2 4 6}

B = {1 3 5 7}



t = (k)T t = (k+1)T t = (k+2)T

FIG. 7

$S_k = (\hat{a}_{k-2}, \hat{a}_{k-1})$ a_k $S_{k+1} = (\hat{a}_{k-1}, \hat{a}_k)$ a_{k+1} $S_{k+2} = (\hat{a}_k, \hat{a}_{k+1})$

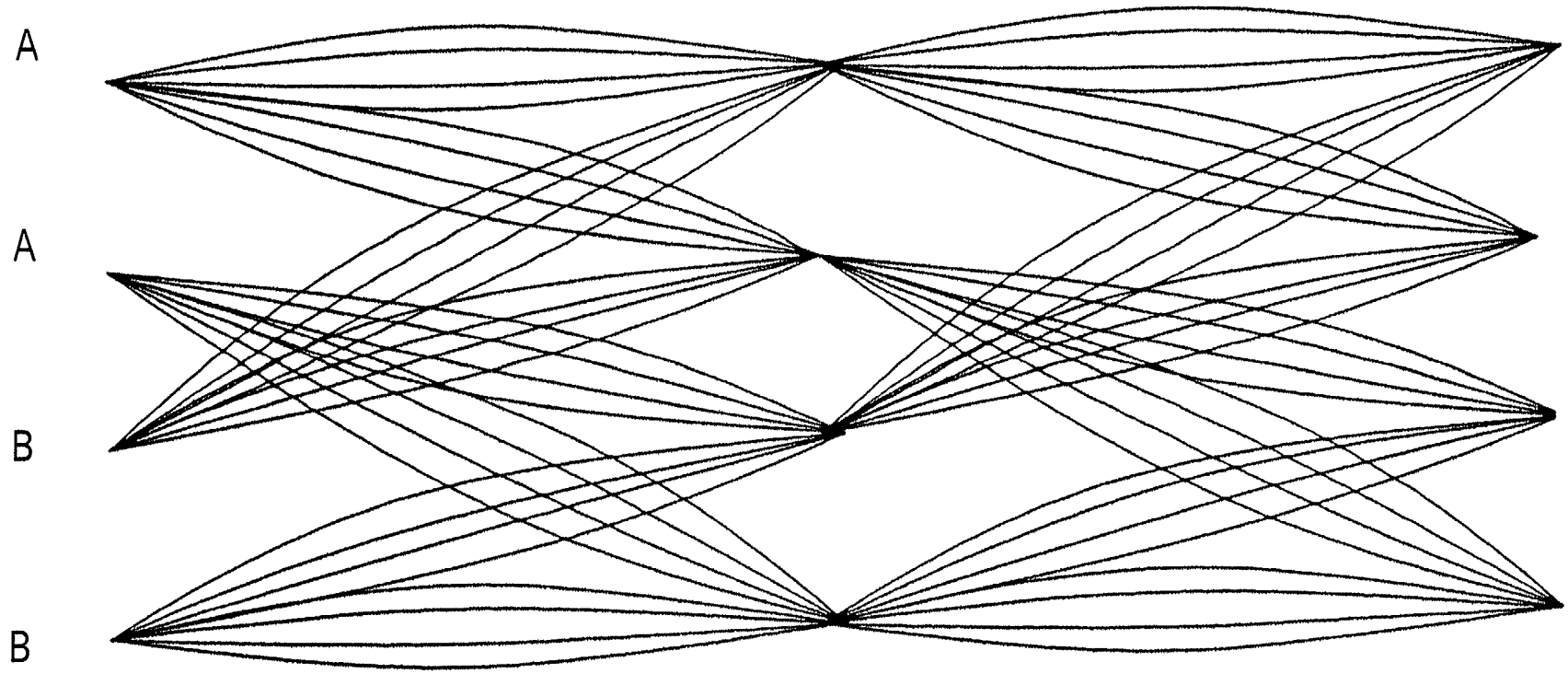


FIG. 8